REMARKS

The present response is filed with a Request for Continued Examination (RCE), and is to the Office Action mailed in the above-referenced case on July 21, 2003, made Final. Claims 1-32 are pending for examination. The Examiner has rejected claims 1-32 under 35 U.S.C. 102(b) as being anticipated by Chang et al. (U.S. 5,634,015), hereinafter Chang.

Applicant has carefully studied the prior art presented by the Examiner, and the Examiner's rejections and statements of the instant Office Action. In response, applicant herein provides further argument to more particularly point out the subject matter of applicant's invention regarded as patentable, and to clearly establish that the reference of Chang fails to anticipate all of applicant's claimed limitations. Applicant points out and argues the key and patentable limitations, which the Examiner appears to have misunderstood or overlooked in his rejections and statements.

Regarding claim 1, the Examiner stated that Chang discloses applicant's method and apparatus for managing a buffer of events in the background, comprising all of the limitations of applicant's claim. The Examiner further stated in the Response to Arguments section of the instant Office Action, that, although passages are found in Chang disclosing some control functions assigned to the processor, the sole responsibility of managing packets/events as they arrive from the network/device belongs to the generic adapter manager (GAM 18), and that GAM 18 controls packet traffic and queue scheduling, and management functions including packet management, queue management, event control and packet traffic control. Applicant respectfully disagrees with the Examiner's statements, and his interpretation of Chang as reading on all of the limitations of applicant's claim. Particularly, applicant traverses the Examiner's above statement pertaining to event control, as there clearly is no

passage anywhere in Chang specifically reciting or dealing with event control. For convenience, applicant reproduces claim 1 below in its present form.

Applicant's claim 1 recites:

1. (Original) A background event buffer manager (BEBM) for ordering and accounting for events in a data processing system having a processor, the BEBM comprising:

a port for receiving event identifications (IDs) from a device;

a queuing function enabled for queuing event IDs received; and

a notification function for notifying the processor of queued event IDs;

characterized in that the BEBM handles all event ordering and accounting for the processor.

Applicant wishes to emphasize the above claim language of "background event buffer manager (BEBM) for ordering and accounting for events", "receiving event identifications (IDs)", "queuing event IDs", "notifying the processor of queued event IDs", and "event ordering and accounting". It is clear from the claim language, and the teaching taken directly from applicant's specification, that it is event IDs, not packets, that are received, queued, identified to the processor, and ordered and accounted for.

In a communication session established over the Internet between any two sites there will be an exchange of a large number of packets. It is important that the packets be received at the destination in the same order as they are generated and transmitted at the source, and, if the source and destination machines were the only two machines involved with the packet flow, and all packets in the flow were to travel by the same path, there would be no problem. Packets would necessarily arrive in the order sent.

However, it is well-known that packets from a source to a destination may flow through a number of machines and systems on the way from source to destination, and there are numerous opportunities for packets to get disordered. Moreover, the machines handling packets at many places in the Internet are dealing with large numbers of sources and destinations, and therefore with a large number of separate packet flows. It is also well known that packets are not necessarily received in a steady flow, but may be received in bursts, and that background memory manager or processor is interrupted for each packet. It is often the case that when the processor is interrupted for packets arriving that the processor is busy on other tasks, and interrupts may arrive in bursts much faster than can be easily handled. In this case the processor has to keep track of all of the events and order the processing of all events. The problems that can occur if the separate packet flows are allowed to be disordered, or arrive faster than the memory manager or processor can handle them, are quite obvious.

Methods and apparatus are provided in applicant's invention for ordering events for a processor other than the order in which data might be received to be processed, and without expenditure of significant processor resources. The system diagram of applicant's Fig. 4 illustrates a system 407 using a Background Event Buffer Manager (BEBM) 401, which works in conjunction with applicant's Background Memory Manager BMM 302, which is a hardware mechanism enabled to manage the packet memory in the background, i.e. with no intervention of the processor to decide where the data structure will be stored in the memory. System 407 in Fig. 4 is a system operating in a packet router, and the network to which input/output device 106 connects is the well-known Internet network.

One goal of the processor is to generate acknowledgements of events as soon as possible to increase the throughput of processed events. The term "events", as used in applicant's specification and claims, refers to the activity of

data packets, such as arrival, sending, and so on. However, the amount of time the processor dedicates to this task can be significant, thus diminishing the performance of the processor on the processing of the events. Moreover, depending on how frequent these events occur, and the amount of processing that each event takes, the processor will not be able to start processing them at the time they occur. Therefore, the processor will need to buffer the events and process them later on. The skilled artisan will surely recognize that the ordering of and accounting for events, as described herein, is a considerable and significant processor load.

In preferred embodiments of applicant's invention, managing of the ordering of the acknowledgements is implemented in hardware and is accomplished in the background (i.e. while the processor is performing the processing of other events). Background Event Buffer Manager (BEBM 401) of applicant's invention, referring now to applicant's Fig. 4, is a system which is at the heart of preferred embodiments of applicant's invention, provided to operate in conjunction with Background Memory Manager (BMM 302), as a convenience adding further advantages in the packet processing system, rather than as a research and on the implementation of BEBM 401.

BEBM 401 buffers, completely in the background, all incoming events, notifies the processor about any event that has been buffered and for which the processor does not know of its existence, updates the status of the acknowledgement for a particular event based on the result of the processing of the event by the processor; and guarantees any of the restrictions imposed on the generation of the acknowledgements with minimal intervention of the processor. BEBM 401 also buffers the transmission of acknowledgements back to the device that generated the events, because the device may be busy with other tasks. As the device becomes capable of processing the acknowledgements, the BEBM sends them to the device.

Applicant now wishes to direct the Examiner's attention to the Abstract portion of Chang, wherein a generic high bandwidth adapter is described, providing a unified architecture for data communications between buses, channels, processors, switch fabrics and/or communication networks, and that, as is known in the art, data is carried by data stream packets of variable lengths, and each packet includes a header control information portion and a data portion. It is further described that a packet memory stores data packets arriving at a generic adapter ports, the packet memory is segmented into buffers, and each data packet is stored in one or more buffers. The generic adapter manager performs and synchronizes management functions, including implementing data structures in the packet memory by organizing data packets in buffers, and organizing data packets into queues. The portion further describes that each generic adapter port has associated therewith a packet memory interface providing for the transfer of data packets into and out of the packet memory, such that when a data packet is received at an input/output port, the data packet is transferred into the adapter packet memory and queued for processing.

Applicant has repeatedly underscored the phrase "data packets" in order to make unmistakably clear to the Examiner that Chang clearly teaches performing data packet management functions, not event management, as is taught and claimed in applicant's invention. Based on the Examiner's remarks in the instant Office Action pertaining to the invention of Chang, it appears that it is the Examiner's position is that, because Chang handles and manages packets, he must also manage packet event identifications (IDs). Applicant argues , however, that this is an incorrect assumption on the Examiner's part.

Applicant has very carefully and thoroughly studied all of the portions of Chang cited and applied by the Examiner, as well as the remainder of the reference, and applicant is certain there is no explicit teaching, suggestion or motivation whatsoever anywhere in the reference for event management, as

taught in applicant's specification and recited in applicant's claims, nor does Chang even discuss packet events.

Applicant argues that Chang teaches an invention for solving a problem which is different from that solved by applicant's invention. The rather common practice of Examiners in rejecting claims because prior art teaches alternative inventions that might accomplish the same or similar purposes does not provide prima facie rejections, and should be discouraged. To create a prima facie rejection, the actual elements of the claimed invention must be shown in the art, and that is clearly not the case in this instance.

One key problem solved by applicant's invention, as stated above by applicant, is that data packets are often arriving at the data packet router, for example, at a much higher rate than they can be processed, and may have different priorities, etc. Applicant's invention solves this problem by providing a system and method for creating, identifying, queuing and ordering events, not data packets as taught in Chang, and notifying the processor of such events as acknowledgements. Applicant strongly believes that this is a key and patentable distinction of applicant's invention over that of Chang, and therefore accordingly deserves patentable weight.

Applicant therefore believes that claim 1, in its present form, distinguishes unarguably over the reference of Chang, as Chang clearly does not disclose all of the limitations of applicant's claim, particularly ordering and accounting for events by receiving, queuing, and acknowledging event IDs. Applicant's independent claims 9 and 17 recite a data processing system and network packet router for practicing applicant's invention as embodied in claim 1, characterized in that the BEBM handles all event ordering and accounting for the processor. Applicant's independent claim 25 recites applicant's method claim in accordance with the independent apparatus claims. The Examiner has rejected claims 9, 17 and 25 using the criteria for the rejection of applicant's claim 1, with the exception of the recitation of "memory coupled to the

processor" in claim 9, stating that Chang discloses this limitation. In view of the above arguments presented by applicant on behalf of claim 1, claims 9, 17 and 25 art then also clearly and unarguably patentable over Chang, and depending claims 2-8, 10-16, 18-24 and 26-32 are then patentable on their own merits, or at least as depended from a patentable claim.

As all of the claims have been shown to be patentable over Chang, applicant respectfully requests that this application be reconsidered, the claims be allowed, and that this case be passed quickly to issue.

If there are any time extensions needed beyond any extension specifically requested with this amendment, such extension of time is hereby requested. If there are any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted,
Mario Nemirovsky et al.

by _____
Donald R. Boys
Reg. No. 35,074

Donald R. Boys
Central Coast Patent Agency
P.O. Box 187
Aromas, CA 95004
(831) 726-1457